REMARKS

Claims 1, 3-9, 12, 14-22 and 25-27 remain in this application. Claims 2, 10, 11, 13, 23 and 24 have been cancelled. Claims 1, 12, 14 and 19-21 have been amended. Claims 25-27 have been added. Claims 1, 12 and 19 are independent claims.

A. Objections to the Specification

In the Office action dated June 1, 2005, objections were made to the specification. Firstly, it was noted that page 9, line 2 included an incorrect reference numeral for the term "the input cell." Applicants have amended the specification to correct the error.

Paragraph [0053] on page 15 of the specification stated "One input 154 of the VCO sets the center frequency (f_O)." The term "f_O" is inconsistent with Figs. 10 and 12, which show the center frequency as "F_O." Paragraph [0053] has been amended to correct the error.

Reconsideration of the objections to the specification is requested.

B. Claim Objections

Claim 12 was objected to for improper recitation of the term "the equalization circuits." Originally, claim 12 identified "equalization circuitry," but not "equalization circuits." As will be described more fully below, claim 12 has been amended to incorporate subject matter from original claim 14, which was dependent upon claim 12. The amended independent claim now states that the equalization circuitry includes equalization circuits.

Reconsideration of claim 12 in view of the amendment to introduce the term "the equalization circuits" is requested.

C. Rejection of the Claims

Claims 1-6, 8-14, 19-20 and 22-24 were rejected under 35 U.S.C. 102(e) as being anticipated by McCormack et al. The remaining claims were rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al. in view of Yiu.

In response to the rejections, Applicants have amended the claims to more clearly distinguish the claimed invention from the cited prior art. Amended claim 1 describes the equalization circuitry as being configured to measure jitter within electrical signals and to utilize jitter measurements as a basis for offsetting transmission losses experienced by electrical signals while external to the claimed crosspoint switch. The equalization circuitry is responsive to the jitter measurements to automatically select levels of equalization. Support for the amendment to claim 1 may be found in original claim 2 and in paragraph [0007] on page 2 of the application as originally filed. Paragraph [0007] states that the first step of the equalization is to measure the jitter and the second step is to tailor the filtering characteristics of the different equalization circuits to minimize the jitter.

In addition to amending claim 1, claims 25, 26 and 27 have been added to be dependent upon claim 1, either directly or indirectly. Claim 25 states that the equalization circuitry includes a multiplexer connected to a jitter measurement component for providing the jitter measurements. The multiplexer is connected to receive electrical signals from each of the input ports and is operatively associated with the jitter measurement component to enable the jitter measurements on a port-by-port basis. Claim 26 states that the jitter measurement component includes a phase-locked loop for tracking data transmissions within the electrical signals and further includes a voltage-controlled oscillator connected to be responsive to the operations of the phase-locked loop. Claim 27 describes the equalization circuitry as being configured to recurringly execute the jitter measurements and the responsive selection of the levels of equalization for individual input ports, thereby enabling the levels of the equalization to track variations in transmission losses. Support for added claims 25-27 may be found in paragraph [0010] on page 3 of the application as originally filed.

Independent claim 12 has been amended to describe the crosspoint switching arrangement as being an integrated circuit having the various components, with the equalization circuitry including a separate equalization circuit for each channel for which equalization is to be applied. Each equalization circuit has a plurality of available configurations of equalization. Support for the amendment may be found in the SUMMARY OF THE INVENTION as originally filed and in original claims 13 and 14.

Independent claim 19 has been amended in a manner consistent with the amendment to claim 1. The amended claim now describes

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the method as including providing on-chip measurements of jitter of electrical signals, wherein the jitter is induced by off-chip conditions. As with claim 1, support for the amendment may be found in paragraphs [0007] and [0010], as well as the description related to the jitter measurement component (142) of Fig. 9.

Applicants respectfully assert that the amendments to the claims place the claims in a condition for allowance.

D. Patentability of Independent Claim 1 and Dependent Claims 3-9

As previously noted, independent claim 1 was rejected under 35 U.S.C. 102(e). To briefly state the standard, rejections under Section 102 are properly only when the claimed subject matter is identically disclosed in a single prior art reference, so that there is no physical difference. In re Marshall, 198 USPQ 344 (CCPA 1978). Claim 1 describes a crosspoint switch integrated circuit. The integrated circuit includes the arrays of input and output ports, the switch matrix, and equalization circuitry. The equalization circuitry of the integrated circuit is configured to measure jitter and to utilize the jitter measurements as the basis for offsetting transmission losses. Applicants assert that McCormack et al. does not teach an integrated circuit, wherein the integrated circuit includes the input and output ports and includes the equalization circuitry configured to measure jitter.

In rejecting claim 2, it was asserted that McCormack et al. discloses equalization circuitry configured to measure jitter. The relevant portions of McCormack et al. were cited as being block 201 in Fig. 1 and paragraphs [0008], [0037], and [0054]. In paragraph [0037], the block 201 is described as being input signal equalization circuits. There is no indication that the input signal equalization circuit should be provided with the capability of measuring jitter. The patent describes access ports (111 and 113) that allow input of programming via a programming interface (109). However, block 201 is not identified as being configured to measure jitter. In the cited paragraph on page 1 of McCormack et al. (i.e., paragraph [0008]), it is merely stated that data degradation may occur due to inter-symbol interference (ISI). An explanation of ISI is provided, but there is no teaching of equalization circuitry configured to measure jitter or to be automatically responsive to jitter measurements.

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Turning to the cited portion of page 4 of McCormack et al. (i.e., paragraph [0054], the prior art reference states that since the passive network includes passive elements, the elements can be segmented and/or programmable. For example, upper metal layers may be changed in order to allow for tuning of a circuit's ISI jitter characteristics. However, the passive network of passive elements does not anticipate equalization circuitry that is configured to measure jitter or to be responsive to jitter measurements to automatically select levels of equalization.

Applicants assert that amended claim 1 is patentably distinguishable from the teachings of McCormack et al. Moreover, even if one were to modify McCormack et al. in view of the teachings of Yiu, the resulting circuit would not render Applicants' claimed invention unpatentable. Yiu is cited primarily with respect to the teaching of equalization to offset "skin effect." Yiu is cited for disclosing switchable connections arranged in electrical parallel, with the components including an inductor and a resistor. It is not asserted that Yiu teaches equalization circuitry within the same integrated circuit as arrays of input and output ports, wherein the equalization circuitry is configured to measure jitter and to be responsive to jitter measurements to automatically select levels of equalization.

Reconsideration of claim 1 and dependent claims 3-9 in view of the amendments is requested.

E. Patentability of Added Claims 25-27

Claims 25-27 describe the structure for providing jitter measurements.

The combination of McCormack et al. and Yiu does not teach or suggest an integrated circuit having equalization circuitry that includes a multiplexer connected to receive electrical signals from each input port, with the multiplexer being operationally associated with a jitter measurement component to enable jitter measurements on a port-by-port basis. Therefore, Applicants submit that claim 25 is patentable over the cited prior art.

The combination of McCormack et al. and Yiu does not teach or suggest a jitter measurement device that includes a phase-locked loop for tracking data transmissions within electrical signals as set forth in claim 25. Nor does the combination of prior art teach or suggest a jitter measurement component that includes a voltage-controlled oscillator configured to be

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responsive to operations of the phase-locked look. Therefore, claim 26 is non-obvious in view of the prior art.

Regarding claim 27, the prior art does not teach or suggest equalization circuitry configured to recurringly execute jitter measurements and recurringly execute the responsive selection of the levels of equalization for individual input ports. It is respectfully submitted that claim 27 is in an allowable condition.

F. Patentability of Claims 19-22

Amended claim 19 describes the method as being one in which equalization is provided for a crosspoint switch formed on an integrated circuit chip. The method includes determining signal characteristics, including providing on-chip measurements of jitter, wherein the jitter is induced by off-chip conditions. Equalization circuitry housed within the crosspoint switch is then set, at least partially based on the on-chip measurements of jitter.

Many of the comments made with regard to the patentability of claim 1 apply equally to the determination of patentability of amended claim 19. The primary reference to McCormack et al. does not anticipate on-chip measuring of jitter. Therefore, McCormack et al. does not anticipate the method described in claim 19. Moreover, it would not be obvious to modify McCormack et al. to include on-chip measuring of jitter and automated setting of equalization circuitry at least partially based on the on-chip jitter measurements. Yiu does not teach such a modification.

Applicants assert that claims 19-22 are allowable over the prior art.

G. Patentability of Claims 12 and 14-18

Claim 12 has been amended to describe the crosspoint switching arrangement as being an integrated circuit having the input ports, the output ports, the switching matrix and the equalization circuitry. The equalization circuitry of the integrated circuit includes a separate equalization circuit for each channel for which equalization is to be applied. As set forth in claim 12, "channels" are connected to the input ports and "channels" are connected to the output ports. For example, the channels connected to the

input ports have non-uniform frequency responses with respect to incoming signal transmissions.

McCormack et al. does not anticipate an integrated circuit that includes equalization circuitry to establish filtering characteristics tailored on the basis of frequency responses of channels that are external to the integrated circuit. McCormack et al. teaches a crosspoint switch unit that includes internal first transmission lines and internal second transmission lines that are orthogonal to the first transmission lines. A switch matrix determines the connection of the first internal transmission lines to the second internal transmission lines. Prior to the first transmission lines, the crosspoint switch unit includes a passive network of capacitors and resistors to compensate for signal degradation. In paragraph [0019], McCormack et al. states "In general terms, the present invention provides a passive network within a signal path before a chain of amplifiers. The passive network has frequency characteristics approximate the inverse of the gain versus the frequency response of the chain of amplifiers over the region that is causing ISI." Applicants submit that the only references to providing compensation for signal degradation that is generated by forces external to the crosspoint switch unit are those involving the location of circuitry external to the crosspoint switches. Thus, paragraph [0055] teaches that if there are multiple stages of crosspoint switches, a passive network of elements may be placed between each of the cascaded crosspoint switch devices in order to reduce signal degradation. This is consistent with [0053] in which it is stated that the passive network may be applied externally to the integrated circuit in order to remove ISI already in fabricated circuits.

In the Section 103(a) rejection, Yiu was cited for teaching the equalization of the frequency response of a transmission line. However, even if one were to modify the teachings of McCormack et al. in view of Yiu, the passive network of capacitors and resistors would continue to be placed between the crosspoint switches as taught by McCormack. The teachings of Yiu do not relate to the positioning of circuitry relevant to a switching matrix of the type described in McCormack et al. or claimed in the pending claims.

Figs. 3, 4A and 8 of Yiu are cited as being relevant. In Fig. 3, a single transmission line is shown. The transmission line is located between a transmitter and a receiver. For purposes of explanation, the transmission line frequency response is modeled by a number of "taps" (36, 42 and 48). These taps of the transmission lines do not teach or suggest the equalization

circuitry or teach a modification of the teachings of McCormack et al. In Fig. 4A, there is a representation of a transfer function which is the inverse of the transmission line transfer function. As described in column 6, lines 27-45 of Yiu, an equalizer may include a number of "taps" that are equivalent to the "taps" of the transmission line as shown in Fig. 3. The number of parallel taps shown in Fig. 8 and the values of the components within each tap depend upon the frequency range that is of interest and the degree of accuracy that is desired. In general, the greater the frequency range and the greater the accuracy, the greater the number of taps that are required. The taps are described as signal processor circuits which each take the input signal from the transmission line and process the signal to mimic a term in the transfer function (column 5, line 58 to column 6, line 2). The signals from the collection of processors/taps are summed and then multiplied by a programmable gain term. Then, the input is added to the output of the multiplier to form an output equalizer signal.

Applicants submit that it would not be obvious to modify McCormack et al. in view of Yiu, since providing the multiple taps (i.e., signal processors) for summing, as shown in Fig. 8, would be cost and space prohibitive if the group of taps needed to be duplicated for each input transmission line of an integrated circuit crosspoint switch.

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited. In the case that any issues regarding this application can be resolved expeditiously via a telephone conversation, Applicants invite the Examiner to call Terry McHugh at (650) 969-8458.

Respectfully submitted,

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